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09/739,141	12/18/2000	Hiroaki Kubo	15162/02970	4838

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EXAMINER	
HANNETT, JAMES M	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,141	KUBO, HIROAKI	
	Examiner	Art Unit	
	James M Hannett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 15-25* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 10/4/2004 have been fully considered but they are not persuasive.

The applicant argues the Nagasaki fails to disclose a temporary memory. The applicant argues that the states three state buffer (17) can not be viewed as a temporary memory.

The examiner disagrees, Nagasaki teaches on Column 4, Lines 31-35 that the three-state buffer controls the digital image signals and then supplies them to the bus at a specific timing. Therefore, the buffering of the image data by the gate circuit (17) is viewed by the examiner as a temporary storage. Therefore, the examiner views the three state buffer to be a temporary memory.

The applicant argues that the prior art does not teach that the image data is copied from the temporary memory to the second memory and then to the first memory. Further more The applicant argues that the prior art does not teach that the second memory can have a higher speed than the first memory.

The examiner disagrees, Nagasaki depicts in Figure 1 the use of a temporary memory (17). Nagasaki teaches that the image data in the temporary memory (17) is transferred to a second memory (34) Column 6, Lines 5-13. Nagasaki teaches that he image data stored in memory (34) is then transferred to a first memory (35) Column 7, lines 16-26. Furthermore, Nagasaki teaches on Column 7, Lines 20-22 that the second memory card (34) has a higher speed than the first memory card (35).

The applicant argues that Nagasaki fails to disclose a controlled that performs a task in parallel with "recording the captured image from the second medium to the first medium".

The examiner disagrees, Nagasaki teaches that the controller (14) controls the operation of the processors (31-33) Nagasaki further teaches that the controller controls the operation of the BUS (18). Nagasaki teaches that he processing functions (31-33) are located on a separate bus so that the camera can increase its operating speeds by allowing one process to use BUS (18) while the processing circuitry uses BUS (36). Therefore, because the controller controls both the operation of the bus (18) and the operation of the processors (31-33) and the tow can operate simultaneously, the controller is able to perform the tow tasks in parallel.

The applicant argues that Nagasaki does not disclose a digital camera that "performs, in parallel, a task of recording the captured image on the first medium and a task of establishing data communication with an external device"

The examiner asserts that claim 24 is independent and is written broadly. Therefore, the examiner has relied upon different memories in Nagasaki in order to meet the claimed limitations. Specifically the claim states that the digital camera has a first memory and a second memory. The examiner views the first memory as memory (37) depicted in Figure 1. Furthermore, the examiner views the second memory as memory card (34). Furthermore, the I/O port of Nagasaki is connected to BUS (18) and memory (37) is connected to bus (36) Nagasaki teaches that this arrangement enables the two processes to perform independently of one another. Therefore, enabling the communication with an external device through I/O port and the processing of the image data and storage into memory (37) to be performed simultaneously.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1: Claims 1-4, 7-12, 17-20 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,153,730 Nagasaki et al.

2: As for Claim 1, Claim 1 is rejected for reasons related to Claim 2, Since Claim 2 is substantively equivalent to Claim 1.

3: In regards to Claim 2, Nagasaki et al depicts in Figure 1 and teaches on Column 4, Lines 20-35, Column 5, Lines 12-27, Column 7, Lines 16-26 a digital camera capable of loading media, comprising: a temporary memory (17) for storing a captured image generated in response to a photographing operation; a first slot capable of loading a first medium (35) for recording and storing said captured image; a second slot capable of loading a second medium (34) for recoding and storing said captured image; and a controller (12) for, when recording said captured image from said temporary memory (17) to said first medium (35) on the condition that said second medium (34) has a higher recording speed than said first medium (35), recording said captured image once from said temporary memory (17) to said second medium (34) and then from said second medium (34) to said first medium (35). The three-state buffer (17) is viewed by the examiner as a temporary memory. Nagasaki et al teaches that the image captured by the image sensor is sent to the buffer memory (17) and is then sent to memory (34); which is viewed by the examiner as the second memory. Thereafter, the CPU transfers the image data from the second memory (34) to the first memory (35) over the BUS (18). Furthermore, Nagasaki et al teaches on

Column 5, Lines 1-2 that the memory cards are detachable. Therefore, it is inherent that the memory cards are connected into slots.

4: As for Claim 3, Claim 3 is rejected for reasons related to Claim 4, Since Claim 4 is substantively equivalent to Claim 3.

5: In regards to Claim 4, Nagasaki et al teaches on Column 6, Lines 5-13 and Column 10, Lines 36-50 that the controller (14) is operable to perform a plurality of tasks in parallel and performs one of said plurality of tasks when recording said captured image from said second medium to said first medium. Nagasaki et al teaches that the camera can transfer the image memory from the second memory to the first memory over the BUS (18). Furthermore, the control circuitry that performs signal processing and data compression can be operated simultaneously in order to increase the speed of the digital camera. Therefore, it is viewed that the camera can perform a plurality of tasks in parallel while transferring the image data from one memory to the other.

6: As for Claim 7, Claim 7 is rejected for reasons related to Claim 8, Since Claim 8 is substantively equivalent to Claim 7.

7: In regards to Claim 8, Nagasaki et al teaches on Column 2, Lines 59-64 and Column 6, Lines 5-13 that when the second medium (34) has enough free space for recording said captured image stored in said temporary memory (17), said controller (14) controls recording processing so that said captured image is recorded once from said temporary memory (17) to said second medium (34) and then from said second medium (34) to said first medium (35).

8: As for Claim 9, Claim 9 is rejected for reasons related to Claim 10, Since Claim 10 is substantively equivalent to Claim 9.

9: In regards to Claim 10, Nagasaki et al depicts in Figure 1 and teaches on Column 4, Lines 20-35, Column 5, Lines 12-27, Column 7, Lines 16-26 a digital camera capable of loading media (34 and 35), comprising: a plurality of slots capable of loading a plurality of media (34 and 35). for recording and storing a captured image generated in response to a photographing operation; and a controller (14) capable of performing a plurality of tasks in parallel. Nagasaki et al teaches on Column 6, Lines 5-13 and Column 10, Lines 36-50 that the controller (14) is operable to perform a plurality of tasks in parallel and performs one of said plurality of tasks when recording said captured image from said second medium to said first medium. Nagasaki et al teaches that the camera can transfer the image memory from the second memory to the first memory over the BUS (18). Furthermore, the control circuitry that performs signal processing and data compression can be operated simultaneously in order to increase the speed of the digital camera. Therefore, it is viewed that the camera can perform a plurality of tasks in parallel while transferring the image data from one memory to the other. Therefore, said controller (14) when performing a first task to record said captured image on a medium (35) which is selected as a subject of recording out of said plurality of media (34 and 35), is viewed by the examiner as transferring the image data from memory (34) to memory (35). Nagasaki et al teaches on Column 5, Lines 1-2 that the memory cards are detachable. Therefore, it is inherent that the memory cards are connected into slots.

10: As for Claim 11, Claim 11 is rejected for reasons related to Claim 12, Since Claim 12 is substantively equivalent to Claim 11.

11: In regards to Claim 12, Nagasaki et al depicts in Figure 7 that the image compression function can utilize a local memory (7) while compressing the data. Furthermore, the data

compression (32) can be performed while image data is transferred under control of the CPU (14) from memory (34) to memory (35).

12: As for Claim 17, Claim 17 is rejected for reasons related to Claim 18, Since Claim 18 is substantively equivalent to Claim 17.

13: In regards to Claim 18, Nagasaki et al teaches on Column 6, Lines 5-13 and Column 10, Lines 36-50 and depicts in Figure 1 that the predetermined processing can be image processing, data compression or digital video processing predetermined processing is image processing on an image recorded on a medium which is not said subject of recording.

14: As for Claim 19, Claim 19 is rejected for reasons related to Claim 20, Since Claim 20 is substantively equivalent to Claim 19.

15: In regards to Claim 20, Nagasaki et al teaches on Column 6, Lines 5-13 and Column 10, Lines 36-50 and depicts in Figure 1 that the predetermined processing can be data compression said image processing is compression processing on said image.

16: In regards to Claim 24, Nagasaki et al depicts in Figure 1 and teaches on Column 4, Lines 20-35, Column 5, Lines 12-27, Column 7, Lines 16-26 a first memory (37) depicted in Figure 1. a second memory (34). Furthermore, the I/O port of Nagasaki is connected to BUS (18) and memory (37) is connected to bus (36). Nagasaki teaches that this arrangement enables the two processes to perform independently of one another. Therefore, enabling the communication with an external device through I/O port and the processing of the image data and storage into memory (37) to be performed simultaneously.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17: Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,153,730 Nagasaki et al in view of USPN 5,067,029 Takahashi.

18: As for Claim 5, Claim 5 is rejected for reasons related to Claim 6, Since Claim 6 is substantively equivalent to Claim 5.

19: In regards to Claim 6, Nagasaki et al teaches on Column 5, Lines 12-27 the use of a first memory and a second memory. Nagasaki et al teaches that the second memory (34) can be SRAM. However, Nagasaki et al teaches that the first memory is EEPROM and does not teach that the first memory can employ magnetic recording.

Takahashi teaches on Column 2, Lines 35-41 and Column 1, Lens 51-56 that it is advantageous when designing a digital camera to use several types of storage medium including an optical storage medium and a magnetic storage medium. This is advantageous because it allows a user to record image data on a recording medium that is compatible with different types of electrical equipment.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the EEPROM memory of Nagasaki et al with a magnetic recording medium in order to allow a user to record image data on a recording medium that is compatible with different types of electrical equipment.

20: Claims 15, 16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,153,730 Nagasaki et al.

21: As for Claim 15, Claim 15 is rejected for reasons related to Claim 16, Since Claim 16 is substantively equivalent to Claim 15.

22: In regards to Claim 16, Nagasaki et al does not teach that the predetermined processing is printing. However, official notice is taken that it was well known in the art at the time the invention was made to allow cameras to output image data to printers in order to generate a hard copy of a desired captured image.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the camera of Nagasaki et al to output the image data to a printer in order to generate a hard copy of a desired captured image.

23: As for Claim 25, Nagasaki et al does not teach that the external device can be a printer. However, official notice is taken that it was well known in the art at the time the invention was made to allow cameras to output image data to printers in order to generate a hard copy of a desired captured image.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable the camera of Nagasaki et al to output the image data to a printer in order to generate a hard copy of a desired captured image.

24: Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,153,730 Nagasaki et al in view of USPN 6,583,893 Satoh et al.

25: As for Claim 21, Nagasaki et al depicts in Figure 1 and teaches on Column 4, Lines 20-35, Column 5, Lines 12-27, Column 7, Lines 16-26 a digital camera capable of loading media,

comprising: a temporary memory (17) for storing a captured image generated in response to a photographing operation; a first slot capable of loading a first medium (35) for recording and storing said captured image; a second slot capable of loading a second medium (34) for recoding and storing said captured image; and a controller (12) for, when recording said captured image from said temporary memory (17) to said first medium (35) on the condition that said second medium (34) has a higher recording speed than said first medium (35), recording said captured image once from said temporary memory (17) to said second medium (34) and then from said second medium (34) to said first medium (35). The three-state buffer (17) is viewed by the examiner as a temporary memory. Nagasaki et al teaches that the image captured by the image sensor is sent to the buffer memory (17) and is then sent to memory (34); which is viewed by the examiner as the second memory. Thereafter, the CPU transfers the image data from the second memory (34) to the first memory (35) over the BUS (18). Nagasaki et al teaches that the camera has a I/O port Used to transmit and receive image data; Column 11, Lines 22-40 to and from an external device. Nagasaki et al teaches on Column 6, Lines 5-13 and Column 10, Lines 36-50 that the controller (14) is operable to perform a plurality of tasks in parallel and performs one of said plurality of tasks when recording said captured image from said second medium to said first medium. Nagasaki et al teaches that the camera can transfer the image memory from the second memory to the first memory over the BUS (18). Furthermore, the control circuitry that performs signal processing and data compression can be operated simultaneously in order to increase the speed of the digital camera. Therefore, it is viewed that the camera can perform a plurality of tasks in parallel while transferring the image data from one memory to the other. Nagasaki et al teaches that the image data can be transferred to a computer and does not teach that the camera

can be directly connected to another camera so that the image data can be transferred to another camera.

Sotoh et al teaches on Column 9, lines 50-60 and depict in Figure 1 a digital camera system in which digital images can be transferred using an I/O port from one camera to another.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the camera of Nagasaki et al to connect to another Digital camera over Its I/O port in order to allow image data to be directly transferred from one camera to another.

26: In regards to Claim 22, Nagasaki et al teaches on Column 11, Lines 22-40 the digital camera comprises a medium (34 and 35) for recording a captured image, and said controller (17) in said first digital camera performs a second task while performing a first task. Nagasaki et al teaches on Column 6, Lines 5-13 and Column 10, Lines 36-50 that the controller (14) is operable to perform a plurality of tasks in parallel and performs one of said plurality of tasks when recording said captured image from said second medium to said first medium. Nagasaki et al teaches that the camera can transfer the image memory from the second memory to the first memory over the BUS (18). Furthermore, the control circuitry that performs signal processing and data compression can be operated simultaneously in order to increase the speed of the digital camera.

27: As for Claim 23, Nagasaki et al teaches the digital camera further comprises first (35) and second (34) media for recording captured image, and said controller (14) in said first digital camera performs said first task to record a captured image on said first medium (35) and performs said second task to transmit said captured image recorded on said second medium to

said second digital camera. Nagasaki et al teaches on Column 6, Lines 5-13 and Column 10, Lines 36-50 that the controller (14) is operable to perform a plurality of tasks in parallel and performs one of said plurality of tasks when recording said captured image from said second medium to said first medium. Nagasaki et al teaches that the camera can transfer the image memory from the second memory to the first memory over the BUS (18). Furthermore, the control circuitry that performs signal processing and data compression can be operated simultaneously in order to increase the speed of the digital camera. Therefore, it is viewed that the camera can perform a plurality of tasks in parallel while transferring the image data from one memory to the other. Nagasaki et al teaches that the camera has an I/O port used to transmit and receive image data to and from an external device; Column 11, Lines 22-40.

Allowable Subject Matter

28: Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M Hannett whose telephone number is 571-272-7309. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2612

JMH
3/17/2005

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